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In re application of :

Yohei KAWABATA et al. : **Attn: BOX PCT**

Serial No. NEW : Docket No. 2001_1871A

Filed December 21, 2001 :

STORAGE-TYPE DATA BROADCAST SERVICE SYSTEM

[Corresponding to PCT/JP01/03300 Filed April 18, 2001]

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents,
Washington, DC 20231

Sir:

Please amend the above-identified application as follows.

In the Specification and Abstract:

Please replace the paragraph beginning at page 9, line 25, with the following rewritten paragraph:

Next, the operation of the component elements of the recoverer 500 shown in FIG. 8 will be described in detail with reference to the above-mentioned FIG. 9. FIG 9 illustrates a process at the time when the packet TSP(n+α) has been inputted, i.e., when PCR(i+1) has been extracted. Hereinafter, a case in which the packet TSP(n) is first inputted to the storage-type data receiving device SDRc shown in FIG. 7 before any other packet TSP belonging to a particular program will be described for convenience.

ATTACHMENT D

Please replace the paragraph beginning at page 12, line 12, with the following rewritten paragraph:

FIG. 9 illustrates the case where the generation frequency of the VCXO 1140 is higher than the appropriate value. In other words, since STC(i-1) is set to be PCR(i-1) as soon as PCR(i-1) is extracted, the control voltage VdP(i-1) applied to the VCXO 1140 is zero. In this case, the frequency F(Vdp(i-1)) of the outputted clock signal SF(Vdp(i-1)) is the reference generation frequency of the VCXO 1140. In other words, the reference generation frequency of the VCXO 1140 is high relative to the PCR of the transport stream TS inputted to the storage-type data receiving device SDRc. As a result, the count number C(Pa(i)/F(Vdp(i)) counted by the system clock counter 1150 during the time interval Pa(i) is greater than the appropriate value.

Please replace the paragraph beginning at page 12, line 25, with the following rewritten paragraph:

As a result, the system clock time T[STC(i)] which is measured during the time interval Pa(i) differs from the reference time T[PCR(i)] by a clock difference ΔP(i). In this example, the system clock time T[STC(i)]" is ahead of the reference time T[PCR(i)], which is originally meant to be identical, by the clock difference ΔP(i). Thus, when the STC which is recovered from the PCR and the PCR before recovery are not in synchronization, the storage-type data receiving device SDRc does not operate properly.

Please replace the paragraph beginning at page 13, line 24, with the following rewritten paragraph:

As a result, the clock difference ΔP(i+1) between the reference time T[PCR(i+1)] and the system clock time T[STC(i+1)]" still has a minus value, although smaller than the previous clock difference ΔP(i).

Please replace the paragraph beginning at page 14, line 9, with the following rewritten paragraph:

Next, the count number C(Pa(i+2)/F(Vdp(i+2)) of the clock signal SF(Vdp(i+2)) as measured by the system clock counter 1150 during the time interval Pa(i+2) from when the packet TSP(n+α+β+γ) is inputted and until PCR(i+2) is extracted is greater than the previous count number C(Pa(i+1)/F(Vdp(i+1)), but smaller than the count number C(Pa(i-1)/F(Vdp(i-1)) corresponding to the reference frequency of the VCXO 1140.

Please replace the paragraph beginning at page 14, line 17, with the following rewritten paragraph:

As a result, the clock difference ΔP(i+2) between the reference time T[PCR(i+2)] and the system clock time T[STC(i+2)]" becomes even smaller than the previous clock difference ΔP(i+1), and takes a plus value. In other words, the system clock time T[STC(i+2)]" is calculated to be slower than the reference time T[PCR(i+2)] by the clock difference ΔP(i+2). This is a result of the generation frequency of the VCXO 1140 being set so as to be smaller than the appropriate value. In this case, the absolute value of the clock difference ΔP(i+2) is smaller than the absolute value of the clock difference ΔP(i+1); thus, dissynchronization between the PCR and the STC is alleviated.

Please replace the paragraph beginning at page 15, line 3, with the following rewritten paragraph:

Based on the plus control voltage VdP(i+2) having a smaller absolute value than that of the control voltage VdP(i+1), the VCXO 1140 outputs as STC(i+2) a clock signal SF(Vdp(i+2)) having a frequency F(Vdp(i+2)) which is slightly greater than the reference generation frequency and greater than the previous frequency F(Vdp(i+1)).

Please replace the paragraph beginning at page 19, line 2, with the following rewritten paragraph:

In other words, the calculated time interval Pc(i) constituting the system clock time T[STC(i)], which is the output from the system clock counter 1150 as expressed by equation (2) above, can be expressed by the following equation (3) in the storage-type digital broadcast service:

$$Pc(i)=C(Pa(i)/F(Vdp(i-1)))/N \quad \cdots\cdots (3)$$

Please replace the paragraph beginning at page 19, line 20, with the following rewritten paragraph:

In order to properly recover the system time clock STC even in this situation, it might be possible to re-generate the PCR in accordance with the actual bit stream transfer rate. However, re-generating the PCR is tantamount to re-encoding the existing transport stream TS itself, which incurs more than negligible cost and time.

Please replace the paragraph beginning at page 22, line 18, with the following rewritten paragraph:

According to a fourth aspect of the present invention based on the first aspect, the receiver comprises:

a PCR extractor for extracting the program clock reference contained in the first transport stream,

a PCRr specifier for causing the PCR extractor to extract as a standard program clock reference the reference clock contained in the first transport stream and contained in packet data transferred at the first transfer rate, and

an STC recoverer for recovering, based on the extracted standard program clock reference, a system time clock which is a processing reference clock for the packet data.

Please replace the paragraph beginning at page 24, line 14, with the following rewritten paragraph:

FIG. 3 is a block diagram schematically illustrating the structure of a transfer rate ratio information appending device for appending TS transfer rate ratio information to a transport stream TS according to the first embodiment of the present invention.

Please replace the paragraph beginning at page 33, line 6, with the following rewritten paragraph:

Next, with reference to FIG. 2, the operation of the STC recoverer 500 will be described. The structure of the STC recoverer 500 is as described above with reference to FIG. 7, and the description thereof is omitted. Although FIG. 2 may appear very similar to FIG. 8, there is a difference in that the cases other than the transfer rate ratio N being 1 are supported in FIG. 2 while the cases other than the transfer rate ratio N being 1 are not contemplated in FIG. 8. Hereinafter, the differences will be mainly described.

Please replace the paragraph beginning at page 35, line 1, with the following rewritten paragraph:

In other words, when the packet TSP(n) is inputted to the storage-type data receiving device SDR1, following the aforementioned processing, the PCR corrector 5020 generates PCRc(i-1) so as to be inputted to the comparator 1100. On the other hand, the controller 260 sets the value of PCRc(i-1)as an initial value for the system clock counter 1150. As a result, STC(i-1) having the same value as PCRc(i-1) is outputted. Thus, by setting the first-detected PCRc value as an initial value for the system clock counter 1150 and performing feedback control based on a difference with respect to PCRc for each i, any adverse effects of PCR being multiplied by K into PCRc can be eliminated.

Please replace the paragraph beginning at page 36, line 3, with the following rewritten paragraph:

As a result, when PCR(i) is extracted from the inputted packet TSP(n+α), i.e., after the lapse of the corrected time interval K · Pa(i) from the extraction of PCR(i-1), the system clock time T[STC(i)] is outputted from the system clock counter 1150. The system clock time T[STC(i)] can be derived from the following equation (5), as a sum of T[STC(i-1)] and a calculated time interval Pc(i), which is defined as the number of pulses of the clock signal SF(Vdp(i-1)) counted during the corrected time interval K · Pa(i):

$$Pc(i)=C(K \cdot Pa(i)/F(Vdp(i-1))) \quad \cdots\cdots (5)$$

Please replace the paragraph beginning at page 37, line 1, with the following rewritten paragraph:

In other words, the system clock time T[STC(i)] which is measured during the corrected time interval K · Pa(i) differs from the corrected reference time T[PCRc(i)] by a clock difference ΔP(i). In this example, the system clock time T[STC(i)]" is ahead of the corrected reference time T[PCRc(i)], which is originally meant to be identical, by the clock difference ΔP(i). Thus, when the STC which is recovered from the PCR (PCRc) and the PCR (PCRc) before recovery are not in synchronization, the storage-type data receiving device SDRc does not properly operate.

Please replace the paragraph beginning at page 37, line 10, with the following rewritten paragraph:

In this situation, since the clock difference ΔP(i) which is outputted from the comparator 1100 has a minus value, the control voltage VdP(i) outputted from the low-pass filter 1130 also has a minus value. Thus, based on the control voltage VdP(i) having a minus value, the generation frequency of the VCXO 1140 is set to be lower than previously. As a result, a clock signal SF(Vdp(i)) having a lower frequency F(Vdp(i)) than the frequency F(Vdp(i-1))

corresponding to the previous, i.e., the control voltage VdP(i-1), is outputted from the VCXO 1140.

Please replace the paragraph beginning at page 37, line 24, with the following rewritten paragraph:

As a result, the clock difference ΔP(i+1) between the corrected reference time T[PCRc(i+1)] and the system clock time T[STC(i+1)]" still has a minus value, although smaller than the previous clock difference ΔP(i).

Please replace the paragraph beginning at page 38, line 15, with the following rewritten paragraph:

As a result, the clock difference ΔP(i+2) between the corrected reference time T[PCRc(i+2)] and the system clock time T[STC(i+2)]" becomes even smaller than the previous clock difference ΔP(i+1), and takes a plus value. In other words, the system clock time T[STC(i+2)]" is calculated to be slower than the corrected reference time T[PCRc(i+2)] by the clock difference ΔP(i+2). This is a result of the generation frequency of the VCXO 1140 being set so as to be smaller than the appropriate value. Note that, in this case, the absolute value of the clock difference ΔP(i+2) is smaller than the absolute value of the clock difference ΔP(i+1); thus, dissynchronization between the PCRc and the STC is alleviated.

Please replace the paragraph beginning at page 39, line 2, with the following rewritten paragraph:

Based on the plus control voltage VdP(i+2) having a smaller absolute value than that of the control voltage VdP(i+1), the VCXO 1140 outputs as STC(i+2) a clock signal SF(Vdp(i+2)) having a frequency F(Vdp(i+2)) which is slightly greater than the reference generation frequency and greater than that of the previous clock signal SF(Vdp(i+1)).

Please replace the paragraph beginning at page 42, line 23, with the following rewritten paragraph:

The transfer rate ratio appender SDS includes a transport stream storage (hereinafter abbreviated as the "TS storage") 10000, a transfer rate ratio inputter 10010, a service information separator (hereinafter abbreviated as the "Si separator") 10020, a descriptor information appender 10030, and a service information remultiplexer (hereinafter abbreviated as the "Si remultiplexer")10040.

Please replace the paragraph beginning at page 53, line 15, with the following rewritten paragraph:

Thus, according to the present invention, when receiving a program which has been transferred particularly slowly in order to be recorded in a recording device, STC can be normally recovered from the program having a slow transfer rate by subjecting the PCR values in the program to factor computation based on transfer rate information which is previously sent from the sending end, or by automatically calculating the transfer rate information at the receiver end. In addition, when reproducing the program from the recording device, program reproduction can be normally performed by using the PCR information appended in the stream of the program as it is.

REMARKS

Kindly enter the above amendments prior to initial examination.

Attached hereto is a marked-up version of the changes made to the specification by the current amendment. The attachment page is captioned "**Version with markings to show changes made**."

Proposed Drawing Amendments are presented herewith under separate cover letter. Approval of these proposed drawing amendments is respectfully requested.

Respectfully submitted,

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corresponding to the number of packets TSP arrayed within the time interval Pa(i).

Similarly, a packet TSP(n+α+β), is located at a time interval Pa(i+1) within 100 ms following the packet TSP(n+α), has assigned thereto an $(i+1)^{th}$ PCR(i+1) which represents its time. That is, PCR(i+1) represents a reference time T[PCR(i)], which falls at a time interval Pa(i+1) after the reference time T[PCR(i)]. β is a natural number corresponding to the number of packets TSP arrayed within the time interval Pa(i+1).

Similarly still, a packet TSP(n+α+β+γ), located at a time interval Pa(i+2) within 100 ms following the packet TSP(n+α+β), has assigned thereto an $(i+2)^{th}$ PCR(i+2), which represents its time. In other words, PCR(i+2) represents a reference time T[PCR(i+2)], which falls at a time interval Pa(i+2) after the reference time T[PCR(i+1)]. γ is a natural number corresponding to the number of packets TSP arrayed within the time interval Pa(i+2).

The relationship between program clock references PCR and packets TSP, which has been described above with respect to the four packets TSP(n) to TSP(n+α+β+γ) belonging to a packet group composing one program, is also true to any packets TSP subsequent to the packet TSP(n+α+β+γ), and is similarly true to the packets TSP belonging to a packet group composing any other program.

Next, the operation of the component elements of the

recoverer 500 shown in FIG. 8 will be described in detail with reference to the above-mentioned FIG. 9. FIG. 8 illustrates a process at the time when the packet TSP(n+α) has been inputted, i.e., when PCR(i+1) has been extracted. Hereinafter, a case in which the packet TSP(n) is first inputted to the storage-type data receiving device SDRc shown in FIG. 7 before any other packet TSP belonging to a particular program will be described for convenience.

When the packet TSP(n) is inputted to the storage-type data receiving device SDRc, the PCR extractor 5010 extracts PCR(i-1) and inputs it to the comparator 1100. On the other hand, the controller 260 shown in FIG. 7 sets the value of PCR(i-1) as an initial value for the system clock counter 1150. As a result, STC(i-1) having the same value as PCR(i-1) is outputted. The time values of a PCR and a system time clock STC are expressed as a reference time T[PCR] and a system clock time T[STC], respectively, as above.

Since the reference time T[PCR(i-1)] and the system clock time T[STC(i-1)] represent the same time, the clock difference ΔP(i-1) which is outputted from the comparator 1100 is zero. As a result, the control voltage VdP(i-1) which is outputted to the VCXO 1140 after the processing by the digital filter 1110, the D/A converter 1120, and the low-pass filter 1130 is a reference voltage (= center-of-control voltage, hereinafter simply referred to as "zero bolts").

.... (2)

where C is a coefficient.

However, if the generation frequency F(Vdp) of the VCXO 1140 is not appropriate, the time interval Pa(i), which is an actual time, and the calculated time interval Pc(i), which is a calculated time, do not match. If a clock signal SF(Vdp) having such an inappropriate frequency is used as an STC, inputted packets TSP cannot be properly processed. Therefore, a feedback control as described below is performed in the STC recoverer 500 in order to recover the STC so as to be accurate with respect to the PCR.

FIG. 9 illustrates the case where the generation frequency of the VCXO 1140 is higher than the appropriate value. In other words, since STC(i-1) is set to be PCR(i-1) as soon as PCR(i-1) is extracted, the control voltage ~~control voltage~~ VdP(i-1) applied to the VCXO 1140 is zero. In this case, the frequency ~~frequency~~ F(Vdp(i-1)) of the outputted clock signal SF(Vdp(i-1)) is the reference generation frequency of the VCXO 1140. In other words, the reference generation frequency of the VCXO 1140 is high relative to the PCR of the transport stream TS inputted to the storage-type data receiving device SDRc. As a result, the count number C(Pa(i)/F(Vdp(i)) counted by the system clock counter 1150 during the time interval Pa(i) is greater than the appropriate value.

As a result, the system clock time T[STC(i)] which is

measured during the time interval Pa(i) differs from the reference time T[PCR(i)] by a clock difference $\Delta P(i)$. In this example, the system clock time T[STC(i)]" is ahead of the reference time T[PCR(i)], which is originally meant to be identical, by the clock difference $\Delta P(i)$. Thus, when the STC which is recovered from the PCR and the PCR before recovery are not in synchronization, the storage-type data receiving device SDRc does not operate properly.

In this situation, since the clock difference $\Delta P(i)$ which is outputted from the comparator 1100 has a minus value, the control voltage VdP(i) outputted from the low-pass filter 1130 is also equal to or less than the reference voltage (hereinafter simply referred to as being "minus"). Thus, based on the control voltage VdP(i) having a minus value, the generation frequency F(Vdp) of the VCXO 1140 is set to be lower than previously. As a result, a clock signal SF(Vdp(i)) having a lower frequency than that of the previous control voltage VdP(i-1) is outputted from the VCXO 1140.

Next, the count number C(Pa(i+1)/F(Vdp(i+1)) of the clock signal SF(Vdp(i+1)) as measured by the system clock counter 1150 during the time interval Pa(i+1) from when the packet TSP(n+$\alpha+\beta$) is inputted and until PCR(i+1) is extracted is smaller than the previous count number C(Pa(i)/F(Vdp(i)).

As a result, the clock difference $\Delta P(i+1)$ between the reference time T[PCR(i+1)] and the system clock time T[STC(i+1)]"

still has a minus value, although smaller than the previous clock difference $\Delta P(i)$.

Therefore, based on the minus control voltage VdP(i+1) having a smaller absolute value than that of the control voltage VdP(i), the VCXO 1140 outputs as STC(i+1) a clock signal SF(Vdp(i+1)) having a frequency F(Vdp) which is smaller than the reference generation frequency but greater than the previous clock signal SF(Vdp(i)).

Next, the count number C(Pa(i+2)/F(Vdp(i+2)) of the clock signal SF(Vdp(i+2)) as measured by the system clock counter 1150 during the time interval Pa(i+2) from when the packet TSP(n+$\alpha+\beta+\gamma$) is inputted and until PCR(i+2) is extracted is greater than the previous count number ~~count number~~ C(Pa(i+1)/F(Vdp(i+1)), but smaller than the count number ~~count number~~ C(Pa(i-1)/F(Vdp(i-1)) corresponding to the reference frequency of the VCXO 1140.

As a result, the clock difference $\Delta P(i+2)$ between the reference time T[PCR(i+2)] and the system clock time T[STC(i+2)]" becomes even smaller than the previous clock difference $\Delta P(i+1)$, and takes a plus value. In other words, the system clock time T[STC(i+2)]" is calculated to be slower than the reference time T[PCR(i+2)] by the clock difference $\Delta P(i+2)$. This is a result of the generation frequency of the VCXO 1140 being set so as to be smaller than the appropriate value. In this case, the absolute value of the clock difference $\Delta P(i+2)$ is smaller than the absolute

value of the clock difference $\triangle P(i+1)$; thus, dissynchronization between the PCR and the STC is alleviated.

Based on the plus control voltage VdP(i+2) having a smaller absolute value than that of the control voltage VdP(i+1), the VCXO 1140 outputs as STC(i+2) a clock signal SF(Vdp(i+2)) having a ~~frequency~~ frequency F(Vdp(i+2)) which is slightly greater than the reference generation frequency and greater than the previous frequency F(Vdp(i+1)).

Through repetitions of the above-described feedback process, the recovered STC follows along the PCR, and the control voltage VdP of VCXO 1140 properly converges until the reference time T[PCR] and the system clock time T[STC] eventually match, so that an STC which is in synchronization with the PCR is recovered.

Thus, in the storage-type data receiving device SDRc, the PCR which was properly read first is set as the initial value of the system clock counter 1150. As a result, even if PCR cannot be properly extracted from the packet TSP, the aforementioned feedback process is valid with subsequent, properly-extracted PCR. Therefore, the recovery of the STC can be continued.

This is effective also in the case where a once-generated transport stream TS is transmitted or received at a time (date/hour) which is different from a scheduled time of generation or transmission/reception. In other words, although the time which is described by PCR(i) is different from the actual time

"transfer rate ratio".

In other words, the calculated time interval Pc(i) constituting the system clock time T[STC(i)], which is the output from the system clock counter 1150 as expressed by equation (2) above, can be expressed by the following equation (3) in the storage-type digital broadcast service:

$$Pc(i)=C(Pa(i)/F(Vdp(i-1)))/N \quad \cdots\cdots (3)$$

Thus, the system clock counter 1150 outputs. In other words, the calculated time interval Pc(i) is not the original time interval Pa(i), but is a count value of the clock signal SF(Vdp(i)) as counted in 1/N of the time interval Pa(i).

Thus, as described above, the only case in which the system clock time T[STC(i)] measured during the time interval Pa(i) differs from the reference time T[PCR(i)] by the clock difference $\triangle P(i)$, i.e., when equation (2) is valid, is when N=1. Therefore, the system time clock STC cannot be properly recovered for any transport stream TS which is transmitted at a bit stream transfer rate other than N=1.

In order to properly recover the system time clock STC even in this situation, it might be possible to re-generate the PCR in accordance with the actual bit stream transfer rate. However, re-generating the PCR is tantamount to re-encoding the existing ~~property~~ transport stream TS itself, which incurs more than negligible cost and time.

a PCR extractor for extracting the program clock reference contained in the first transport stream,

an STC recoverer for recovering, based on the extracted program clock reference, a system time clock which is a processing reference clock for the packet data,

an STC/PCR rate ratio calculator for deriving, based on the extracted program clock reference and the recovered system time clock, a correction factor for correcting the extracted program clock reference so as to match the second transfer rate, and

a PCR corrector for correcting the extracted program clock reference based on the correction factor, wherein the STC recoverer is feedback-controlled to recover a system time clock based on the corrected program clock reference.

Thus, according to the third aspect, there is no need to re-encode the first transport stream in accordance with the transfer rate.

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According to a fourth aspect of the present invention based on the first aspect, ~~the storage-type data broadcast service system according to claim 1, wherein~~ the receiver comprises:

a PCR extractor for extracting the program clock reference contained in the first transport stream,

a PCRr specifier for causing the PCR extractor to extract as a standard program clock reference the reference clock contained in the first transport stream and contained in packet

data transferred at the first transfer rate, and

an STC recoverer for recovering, based on the extracted standard program clock reference, a system time clock which is a processing reference clock for the packet data.

Thus, according to the fourth aspect, there is no need to re-encode the first transport stream in accordance with the transfer rate.

According to a fifth aspect of the present invention based on the first aspect, the transmitter comprises a transfer rate ratio appender for assigning the transfer rate ratio to the first transport stream TS, and

wherein the receiver comprises:

a PCR extractor for extracting the program clock reference contained in the first transport stream,

an STC recoverer for recovering, based on the extracted program clock reference, a system time clock which is a processing reference clock for the packet data,

a PCR correction factor generator for extracting the transfer rate ratio from the first transport stream, and deriving, based on the extracted transfer rate ratio, a correction factor for correcting the extracted program clock reference so as to match the second transfer rate, and

a PCR corrector for correcting the extracted program clock reference based on the correction factor, wherein the STC recoverer is feedback-controlled to recover a system time clock

based on the corrected program clock reference.

Thus, according to the fifth aspect, the first transport stream has assigned thereto a transfer rate ratio, so that the system time clock can be properly recovered even if the extraction of the program clock reference fails.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram schematically illustrating the structure of a storage-type data receiving device according to a first embodiment of the present invention.

FIG. 2 is an explanatory diagram illustrating a relationship between a program clock reference and a system time clock in the storage-type data receiving device shown in FIG. 1.

FIG. 3 is a block diagram schematically illustrating the structure of a transfer rate ratio information appending device for appending ~~a transport stream~~ TS transfer rate ratio information to a transport stream TS according to the first embodiment of the present invention.

FIG. 4 is a block diagram schematically illustrating the structure of a storage-type data receiving device according to a second embodiment of the present invention.

FIG. 5 is a block diagram schematically illustrating the structure of a storage-type data receiving device according to a third embodiment of the present invention.

FIG. 6 is a block diagram schematically illustrating

The PCR corrector 5020 corrects the PCR inputted from the PCR extractor 5010 with the correction factor K inputted from the STC recoverer 500. Specifically, the value of the PCR is multiplied by K to generate the corrected program clock reference PCRc.

Next, with reference to FIG. 2, the operation of the STC recoverer 500 will be described. The structure of the STC recoverer 500 is as described above with reference to FIG. 7, and the description thereof is omitted. Although FIG. 2 may appear very similar to FIG. 8, there is a difference in that the cases other than the transfer rate ratio N being 1 are supported in FIG. 2 while the cases other than the transfer rate ratio N being 1 are not contemplated in FIG. 8. Hereinafter, the differences will be mainly described.

As already described, an n^{th} packet TSP(n) among all packets TSP belonging to the same program that are contained in the transport stream TS contains time information concerning an $(i-1)^{th}$ PCR(i-1). A packet TSP(n+α), located at a time interval Pa(i) within 100 ms following the packet TSP(n) containing PCR(i-1), has an i^{th} PCR(i) assigned thereto which represents its time. PCR(i) is originally supposed to represent a reference time T[PCR(i)], which falls at a time interval Pa(i) after the reference time T[PCR(i-1)]. However, in the case where the transport stream TS is being transmitted or received at the transfer rate ratio N, PCR(i) represents a corrected reference

In other words, when the packet TSP(n) is inputted to the storage-type data receiving device SDR1, following the aforementioned processing, the PCR corrector 5020 generates PCRc(i-1) so as to be inputted to the comparator 1100.

On the other hand, the controller 260 sets the value of PCRc(i-1) as an initial value for the system clock counter 1150. As a result, STC(i-1) having the same value as PCRc(i-1) is outputted. Thus, by setting the first-detected PCRc value as an initial value for the system clock counter 1150 and performing feedback control based on a difference with respect to PCRc for each i, any adverse effects of PCR being multiplied by K into PCRc can be eliminated.

Therefore, the clock difference $\Delta P(i-1)$ which is outputted from the comparator 1100 is zero. As a result, the control voltage VdP(i-1) which is outputted to the VCXO 1140 after being subjected to the processing by the digital filter 1110, the D/A converter 1120, and the low-pass filter 1130 is zero bolts.

Thereafter, from the VCXO 1140, a clock signal SF(Vdp(i-1)) which is oscillated at the initially-set clock of (27 MHz) of the VCXO 1140, is outputted to the system clock counter 1150, and is also outputted to the program extractor 210 as an STC, at the corrected reference time T[PCRc(i-1)].

The system clock counter 1150 consecutively counts pulses of the inputted clock signal SF(Vdp(i-1)) and accumulates the count values to the initially-set time of PCR(i-1), and consecutively generates a system clock time T[STC], which is the

time represented by STC, for being outputted to the digital filter 1110.

As a result, when PCR(i) is extracted from the inputted packet TSP(n+α), i.e., after the lapse of the corrected time interval K·Pa(i) from the extraction of PCR(i-1), the system clock time T[STC(i)] is outputted from the system clock counter 1150. The system clock time T[STC(i)] can be derived from the following equation (5), as a sum of T[STC(i-1)] and a calculated time interval Pc(i), which is defined as the number of pulses of the clock signal SF(Vdp(i-1)) counted during the corrected time interval K·Pa(i):

$$Pc(i)=C(K\cdot Pa(i)/F(Vdp(i-1))) \quad \cdots\cdots (5)$$

FIG. 2 illustrates the case where the generation frequency of the VCXO 1140 is higher than the appropriate value. In other words, since STC(i-1) is set to be PCRc(i-1) as soon as PCRc(i-1) is extracted, the control voltage VdP(i-1) for the VCXO 1140 is zero. In this case, the frequency clock signal F(Vdp(i-1)) of the outputted clock signal SF(Vdp(i-1)) is the reference generation frequency (e.g., 27 MHz) of the VCXO 1140. The reference generation frequency of the VCXO 1140 is high relative to the PCR of the transport stream TS inputted to the storage-type data receiving device SDR1. As a result, the count number C(K·Pa(i)/F(Vdp(i))) counted by the system clock counter 1150 during the corrected time interval K·Pa(i) is greater than the appropriate value.

In other words, the system clock time T[STC(i)] which is measured during the corrected time interval K·Pa(i) differs from the corrected reference time T[PCR$_A^c$(i)] by a clock difference △P(i). In this example, the system clock time T[STC(i)]" is ahead of the corrected reference time T[PCR$_A^c$(i)], which is originally meant to be identical, by the clock difference △P(i). Thus, when the STC which is recovered from the PCR (PCRc) and the PCR (PCRc) before recovery are not in synchronization, the storage-type data receiving device SDRc does not properly operate.

In this situation, since the clock difference △P(i) which is outputted from the comparator 1100 has a minus value, the control voltage VdP(i) outputted from the low-pass filter 1130 also has a minus value. Thus, based on the control voltage VdP(i) having a minus value, the generation frequency of the VCXO 1140 is set to be lower than previously. As a result, a clock signal SF(Vdp(i)) having a lower ~~frequency~~ frequency F(Vdp(i)) than the frequency F(Vdp(i-1)) corresponding to the previous, i.e., the control voltage VdP(i-1), is outputted from the VCXO 1140.

Next, the count number C(K·Pa(i+1)/F(Vdp(i+1)) of the clock signal SF(Vdp(i+1)) as measured by the system clock counter 1150 during the corrected time interval K·Pa(i) from when the packet TSP(n+α+β) is inputted and until PCR(i+1) is extracted is smaller than the previous count number C(K·Pa/F(Vdp(i)).

As a result, the clock difference △P(i+1) between the corrected reference time T[PCRc(i+1)] and the system clock time

T[STC(i+1)]" still has a minus value, although smaller than the previous clock difference $\Delta P(i)$.

Therefore, based on the minus control voltage VdP(i+1) having a smaller absolute value than that of the control voltage VdP(i), the VCXO 1140 outputs as STC(i+1) a clock signal SF(Vdp(i+1)) having a frequency F(Vdp+1) which is smaller than the reference generation frequency (27 MHz) but greater than the previous frequency F(Vdp(i)).

Next, the count number C(K·Pa(i+2)/F(Vdp(i+2)) of the clock signal SF(Vdp(i+2)) as measured by the system clock counter 1150 during the corrected time interval K·Pa(i+2) from when the packet TSP($n+\alpha+\beta+\gamma$) is inputted and until PCR(i+2) is extracted is smaller than the previous count number C(K · Pa(i+1)/F(Vdp(i+1)).

As a result, the clock difference $\Delta P(i+2)$ between the corrected reference time T[PCRc(i+2)] and the system clock time T[STC(i+2)]" becomes even smaller than the previous clock difference $\Delta P(i+1)$, and takes a plus value. In other words, the system clock time T[STC(i+2)]" is calculated to be slower than the corrected reference time T[PCRc(i+2)] by the clock difference $\Delta P(i+2)$. This is a result of the generation frequency of the VCXO 1140 being set so as to be smaller than the appropriate value. Note that, in this case, the absolute value of the clock difference $\Delta P(i+2)$ is smaller than the absolute value of the clock difference $\Delta P(i+1)$; thus, dissynchronization between the PCRc and the STC

is alleviated.

Based on the plus control voltage VdP(i+2) having a smaller absolute value than that of the control voltage VdP(i+1), the VCXO 1140 outputs as STC(i+2) a clock signal SF(Vdp(i+2)) having a frequency F(Vdp(i+2)) which is slightly greater than the reference generation frequency and greater than that of the previous clock signal SF(Vdp(i+1)).

Through repetitions of the above-described feedback process, the recovered STC follows along the corrected program clock reference PCRc (i.e., the program clock reference PCR), and the control voltage VdP of VCXO 1140 properly converges until the corrected reference time T[PCRc] and the system clock time T[STC] eventually match. In other words, the reference time T[PCR] and the system clock time T[STC] match, so that an STC which is in synchronization with the PCR is recovered.

Thus, in the storage-type data receiving device SDR1 according to the present invention, by correcting PCR(i) based on the transfer rate ratio N of the transport stream TS, the system time clock STC can be properly recovered based on the original PCR even in cases other than the transfer rate ratio N being 1. Moreover, by setting PCRc(i) which is generated from the PCR(i) which was properly read first as the initial value of the system clock counter 1150, even if PCR cannot be properly extracted from the packet TSP, the aforementioned feedback process is valid with subsequent, properly-extracted PCR. Therefore, the recovery of

scheduled time of generation or transmission/reception, or from the secondary transport stream TSs which is once recorded and stored.

As described above, according to the present embodiment, STC recovery can be normally performed even when receiving a program which has been transferred at a non-standard transfer rate (i.e., the transfer rate ratio N not being 1). When reproducing the program from the data storage 200, program reproduction can be normally performed by using the PCR information appended in the stream of the program as it is.

If the extraction of the program clock reference PCR fails due to problems related to the transfer path and the like, it would conventionally be impossible to recover the system time clock STC even when the transfer rate ratio N is 1 because of absence of a feedback process between two contiguous PCR's. Even in such cases, according to the present embodiment, it is possible to perform a feedback process between a recently-extracted PCR and a currently-extracted PCR, based on the transfer rate ratio N which is assigned to the transport stream TS.

Next, with reference to FIG. 3, a transfer rate ratio appender SDS for embedding a transfer rate ratio N in a transport stream TS for use at the transmitter end will be described.

The transfer rate ratio appender SDS includes a transport stream storage (hereinafter abbreviated as the "TS storage") 10009, a transfer rate ratio inputter 10010, a service

information separator (hereinafter abbreviated as the "Si separator") 10020, a descriptor information appender 10030, and a ~~difference~~ service information remultiplexer (hereinafter abbreviated as the "Si remultiplexer")10040.

The TS storage 10000, which is composed of a hard disk or the like, stores the transport stream TS prior to transmission. The transfer rate ratio inputter 10010 inputs a transfer rate ratio N used when the transmission end actually transmits the transport stream TS.

The transfer rate ratio inputter 10010 inputs the transfer rate ratio N as instructed at the transmission end to the TS storage 10000 and the descriptor information appender 10030. The TS storage 10000 outputs the stored transport stream TS to the Si separator 10020 and the Si remultiplexer 10040 at the transfer rate ratio N as instructed.

The Si separator 10020 extracts region data which is open to users, e.g., a PMT (Program Map Table) or an EIT (Event Information Table), which are among the service information Si of the inputted transport stream TS'. The present specification illustrates the case where PMT is the region data. In other words, the Si separator 10020 extracts PMT from the transport stream TS and outputs it to the descriptor information appender 10030.

To the PMT inputted from the Si separator 10020, the descriptor information appender 10030 writes the transfer rate ratio N inputted from the transfer rate ratio inputter 10010,

to the STC recoverer 500.

Thus, in the present embodiment, PCR information (standard program clock references PCRr) which is appended to another program which is being transferred at a standard transfer rate as specified by the PCRr specifier 8000 is extracted. Then, the STC recoverer 500 performs STC recovery by using the PCR (PCRr) value of the other program which is being sent at a normal transfer rate, rather than the PCR of the program to be recorded (i.e., the transfer rate ratio N not being 1).

As a result, STC can be normally recovered from a program having a non-standard transfer rate, and when reproducing the program from the data storage 200, program reproduction can be normally performed by using the PCR information appended in the stream of the program as it is.

Thus, according to the present invention, when receiving a program which has been transferred particularly slowly in order to be recorded in a recording device, STC can be normally recovered from the program having a slow transfer rate by subjecting the PCR values in the program to factor computation based on transfer rate ~~cost~~ information which is previously sent from the sending end, or by automatically calculating the transfer rate ~~cost~~ information at the receiver end. In addition, when reproducing the program from the recording device, program reproduction can be normally performed by using the PCR information appended in the stream of the program as it is.

THE COMMISSIONER IS AUTHORIZED
TO CHARGE ANY DEFICIENCY IN THE
FEES FOR THIS PAPER TO DEPOSIT
ACCOUNT NO 23-0975

10/018752
531 Rec'd PCT/ 21 DEC 2001

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of :

Yohei KAWABATA et al. : **Attn: BOX PCT**

Serial No. NEW : Docket No. 2001_1871A

Filed December 21, 2001 :

STORAGE-TYPE DATA BROADCAST
SERVICE SYSTEM

Corresponding to PCT/JP01/03300
Filed April 18, 2001]

LETTER RE PROPOSED DRAWING AMENDMENTS

Assistant Commissioner for Patents,
Washington, D.C.

Sir:

Enclosed herewith is a photocopy of Figs. 5 and 7-9 marked in red to indicate proposed drawing amendments thereto.

The Examiner is requested to approve such proposed drawing amendments, and after allowance of this application, formal drawings incorporating such amendments will be filed.

Respectfully submitted,

Yohei KAWABATA et al.

By _____
Charles R. Watts
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December 21, 2001

FIG. 5

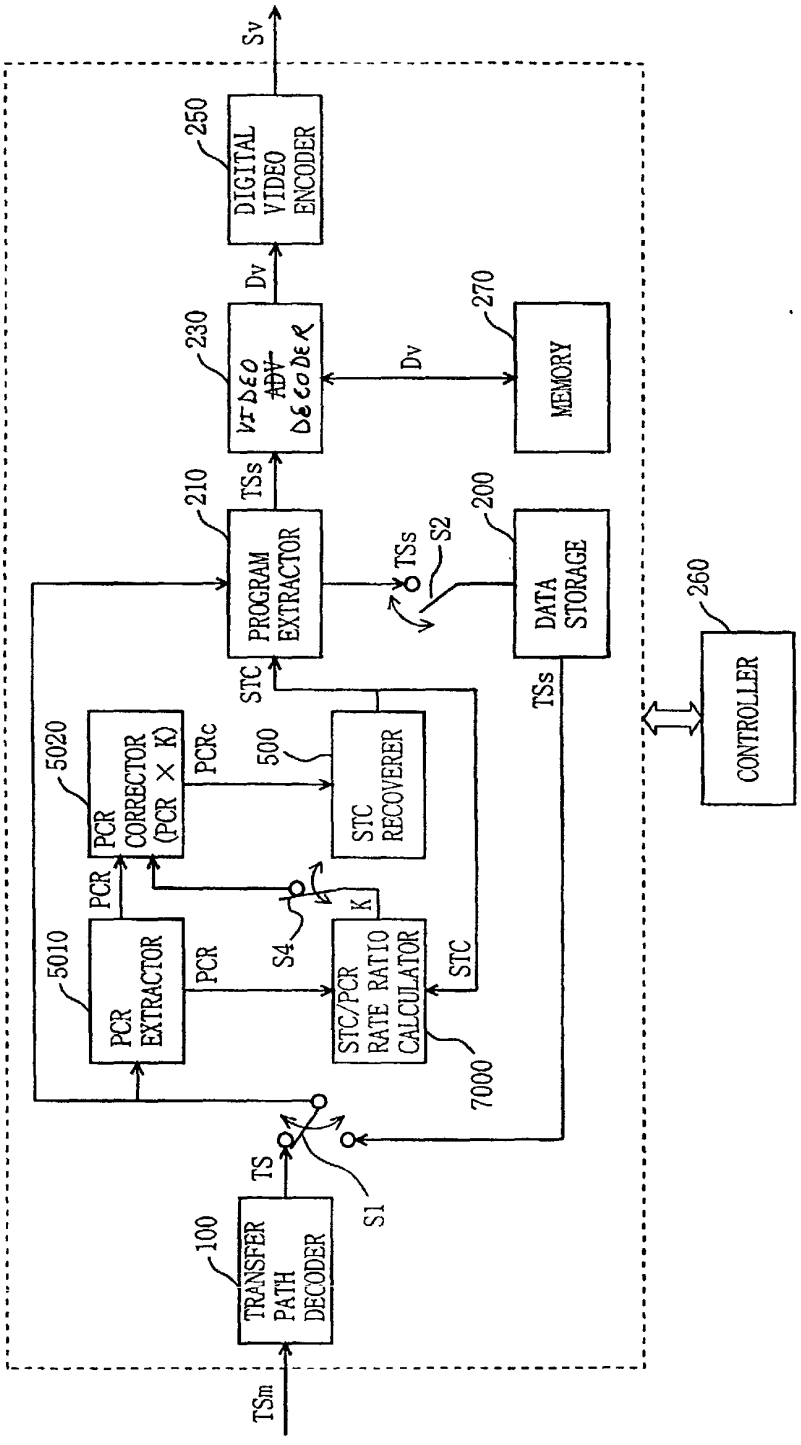

SDR3
TSm
TRANSFER PATH DECODER
100
TS
S1
PCR EXTRACTOR
5010
PCR
S4
STC/PCR RATE RATIO CALCULATOR
K
STC
7000
PCR CORRECTOR (PCR × K)
5020
PCRc
500
STC RECOVERER
STC
PROGRAM EXTRACTOR
210
TSs
S2
DATA STORAGE
200
TSs
VIDEO ADV DECODER
230
Dv
MEMORY
270
DIGITAL VIDEO ENCODER
250
Sv
CONTROLLER
260

FIG. 7 - PRIOR ART

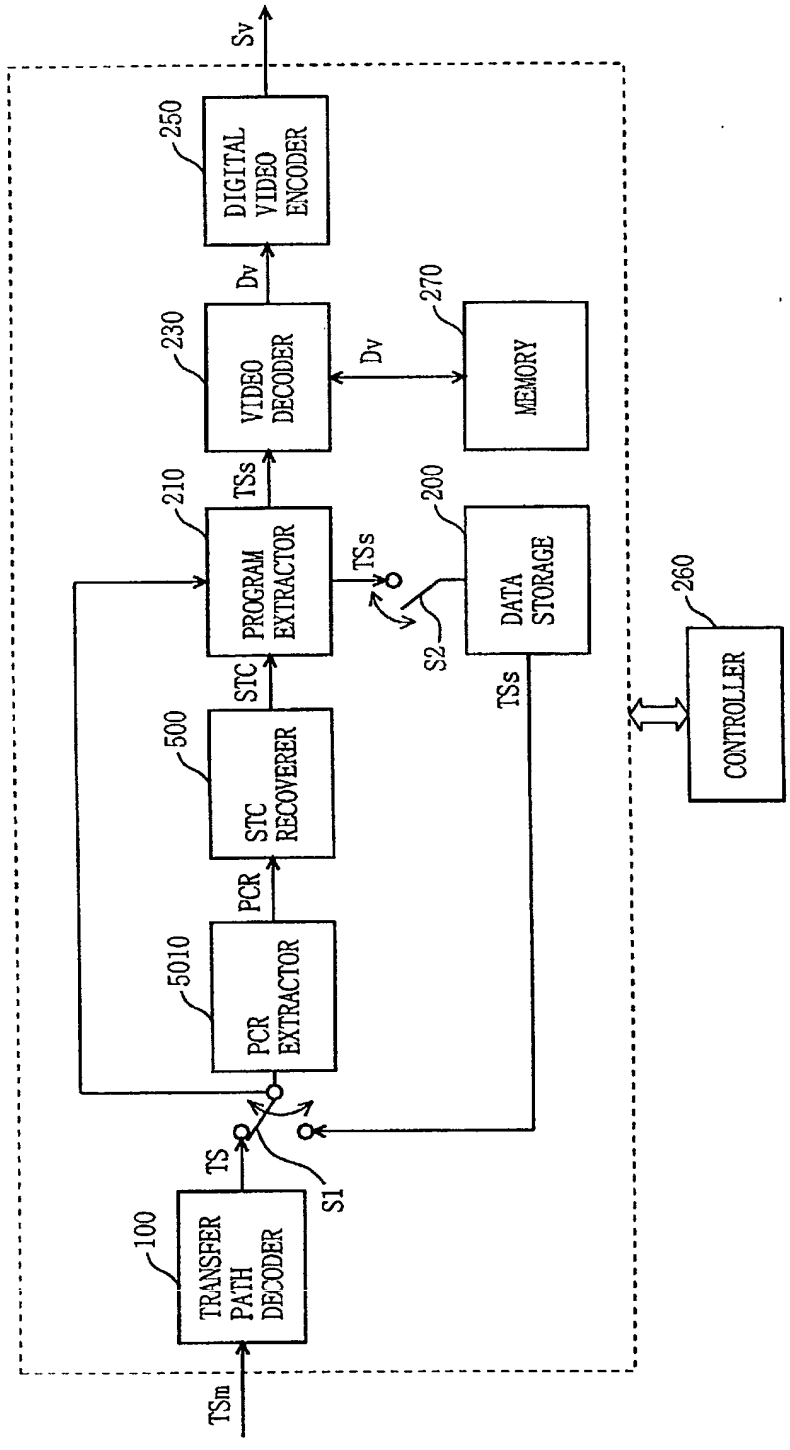
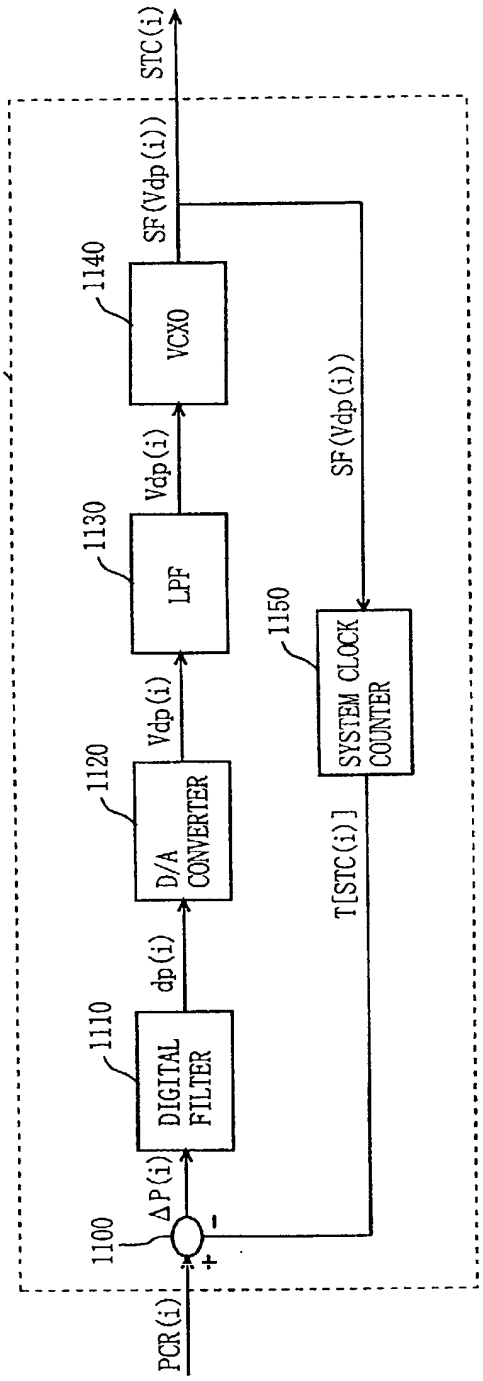


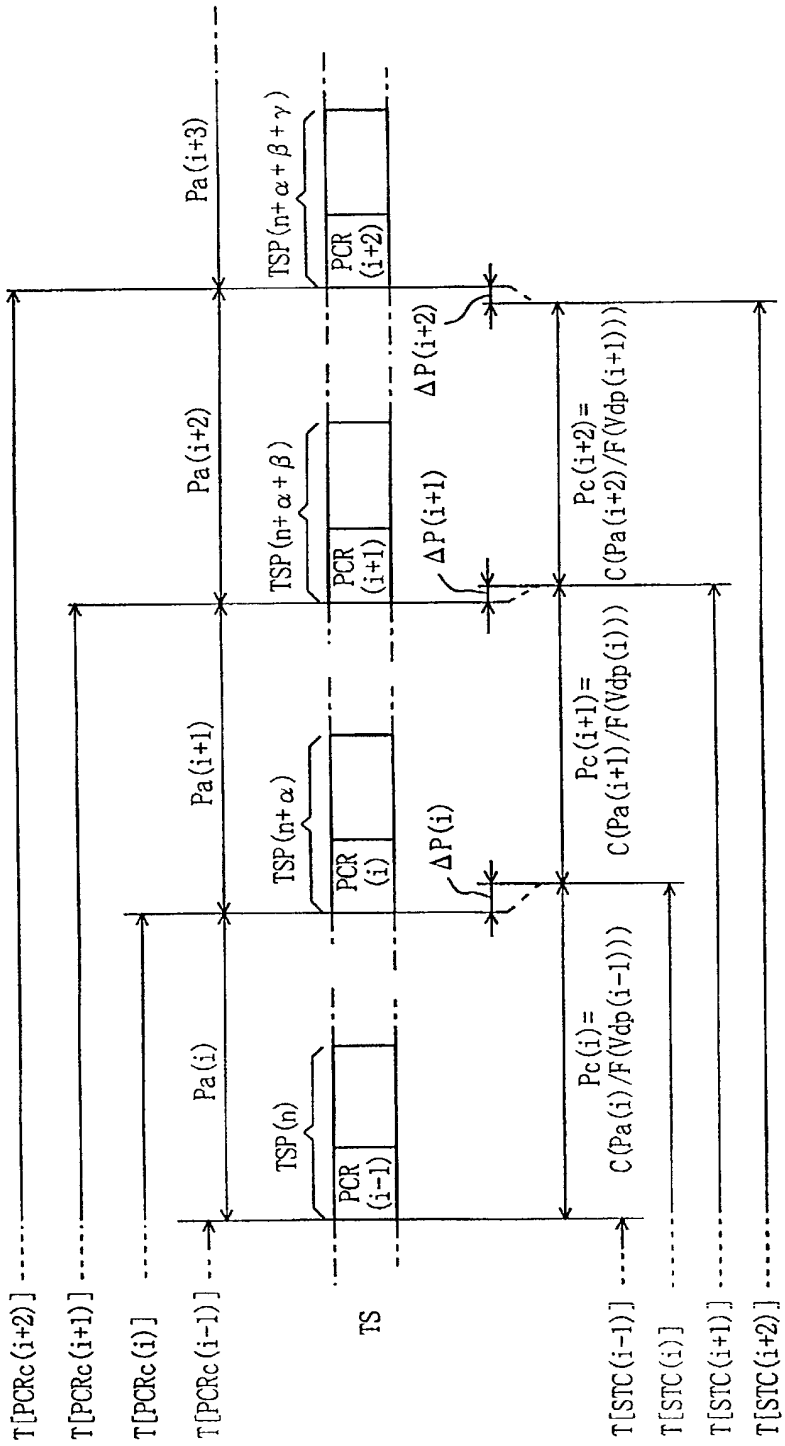
FIG. 8 - PRIOR ART



$T[STC(i)] = T[STC(i-1)] + Pc(i)$

$Pc(i) = C(Pa(i)/F(Vdp(i-1))$

FIG. 9 - PRIOR ART



10/018752

10 Rec'd PCT/PTO 13 MAR 2002

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	:	**Confirmation No. 2619**
Yohei KAWABATA et al.	:	**Attn: BOX PCT**
Serial No. 10/018,752	:	**Docket No. 2001_1871A**
Filed December 21, 2001	:	

STORAGE-TYPE DATA BROADCAST SERVICE SYSTEM
[Corresponding to PCT/JP01/03300 Filed April 18, 2000]

SUBMISSION OF SUBSTITUTE FORMAL DRAWINGS

Assistant Commissioner for Patents,
Washington, DC 20231

THE COMMISSIONER IS AUTHORIZED TO CHARGE ANY DEFICIENCY IN THE FEES FOR THIS PAPER TO DEPOSIT ACCOUNT NO. 23-0975

Sir:

Substitute formal drawings are enclosed. These drawings incorporate the proposed drawing amendments submitted on December 21, 2001.

Respectfully submitted,

Yohei KAWABATA et al.

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Attorney for Applicants

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March 13, 2002

FIG. 1

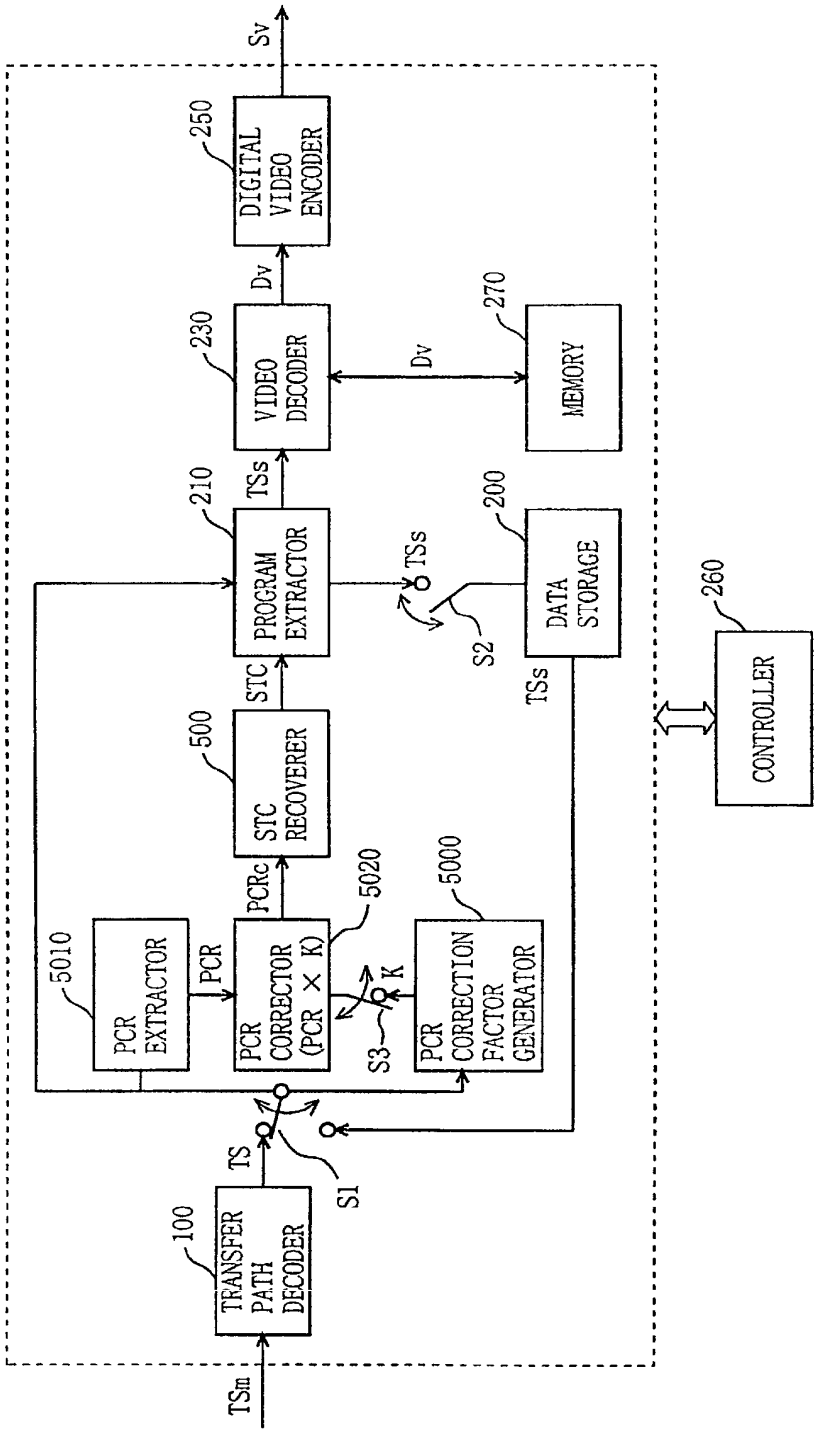

SDR1
TSm
TRANSFER PATH DECODER
100
TS
S1
PCR EXTRACTOR
5010
PCR
PCR CORRECTOR (PCR × K)
5020
PCRc
K
S3
PCR CORRECTION FACTOR GENERATOR
5000
STC RECOVERER
500
STC
PROGRAM EXTRACTOR
210
TSs
S2
DATA STORAGE
200
TSs
CONTROLLER
260
VIDEO DECODER
230
Dv
MEMORY
270
Dv
DIGITAL VIDEO ENCODER
250
Sv

FIG. 2

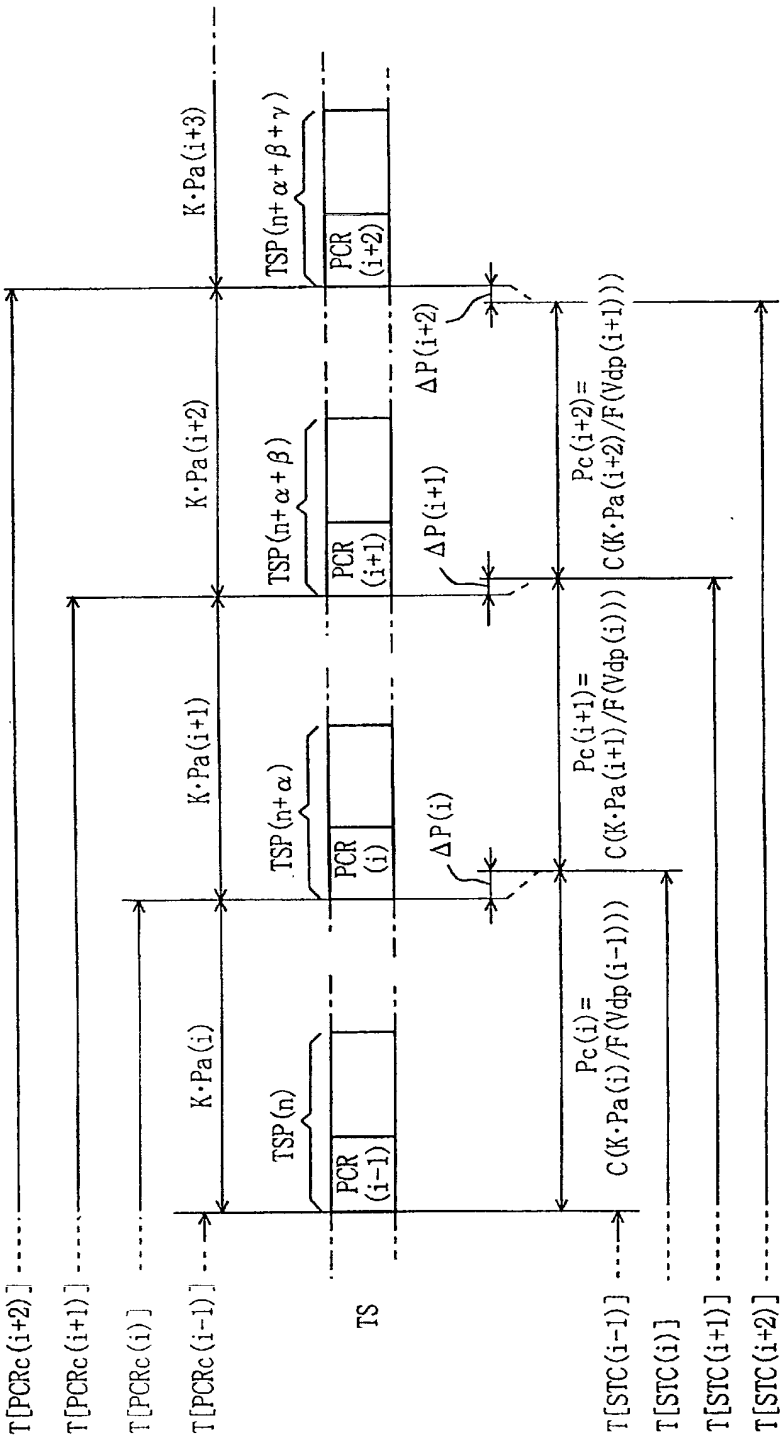

T[PCRc(i+2)]
T[PCRc(i+1)]
T[PCRc(i)]
T[PCRc(i-1)]
K·Pa(i+3)
K·Pa(i+2)
K·Pa(i+1)
K·Pa(i)
TSP(n+α+β+γ)
TSP(n+α+β)
TSP(n+α)
TSP(n)
PCR (i+2)
PCR (i+1)
PCR (i)
PCR (i-1)
ΔP(i+2)
ΔP(i+1)
ΔP(i)
Pc(i+2)= C(K·Pa(i+2)/F(Vdp(i+1)))
Pc(i+1)= C(K·Pa(i+1)/F(Vdp(i)))
Pc(i)= C(K·Pa(i)/F(Vdp(i-1)))
TS
T[STC(i-1)]
T[STC(i)]
T[STC(i+1)]
T[STC(i+2)]

FIG. 3

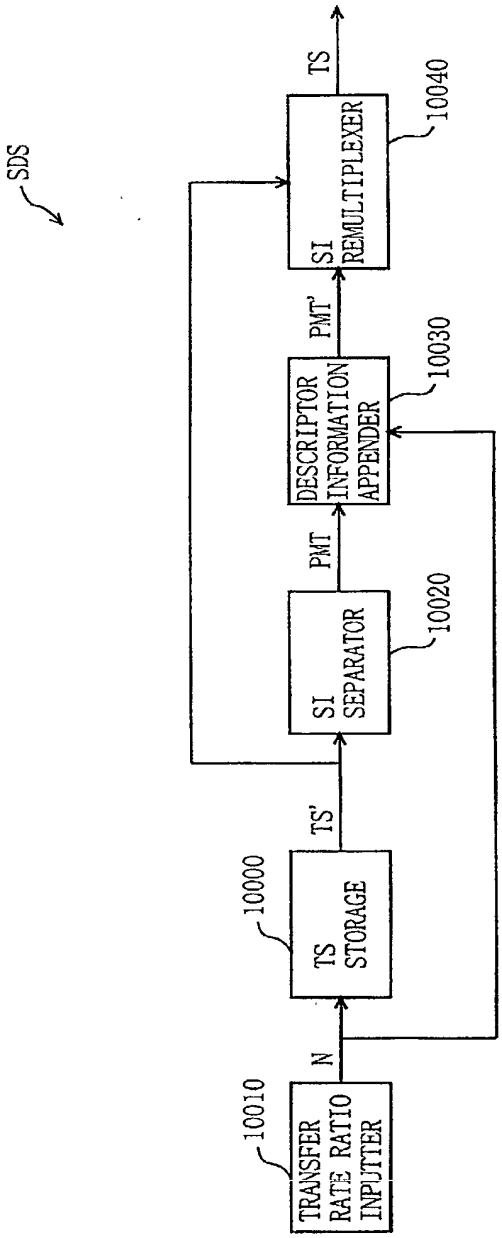

SDS
TRANSFER RATE RATIO INPUTTER
10010
N
TS STORAGE
10000
TS'
SI SEPARATOR
10020
PMT
DESCRIPTOR INFORMATION APPENDER
10030
PMT'
SI REMULTIPLEXER
10040
TS

FIG. 4

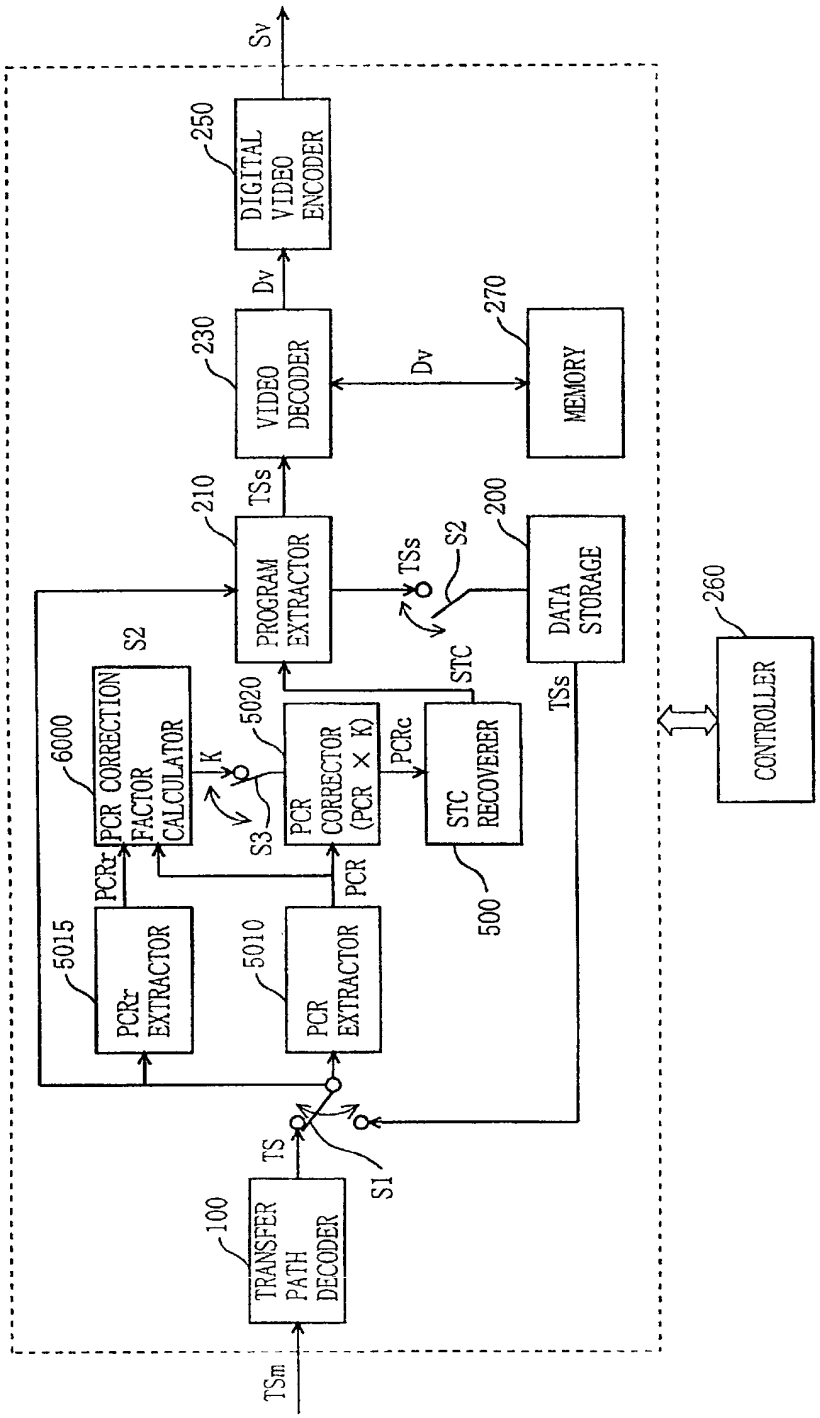

SDR2
TSm
TRANSFER PATH DECODER
100
TS
S1
PCRr EXTRACTOR
5015
PCR EXTRACTOR
5010
PCRr
PCR
PCR CORRECTION FACTOR CALCULATOR
6000
S2
K
S3
PCR CORRECTOR (PCR × K)
5020
PCRc
STC RECOVERER
500
STC
PROGRAM EXTRACTOR
210
TSs
S2
DATA STORAGE
200
TSs
VIDEO DECODER
230
Dv
MEMORY
270
Dv
DIGITAL VIDEO ENCODER
250
Sv
CONTROLLER
260

FIG. 5

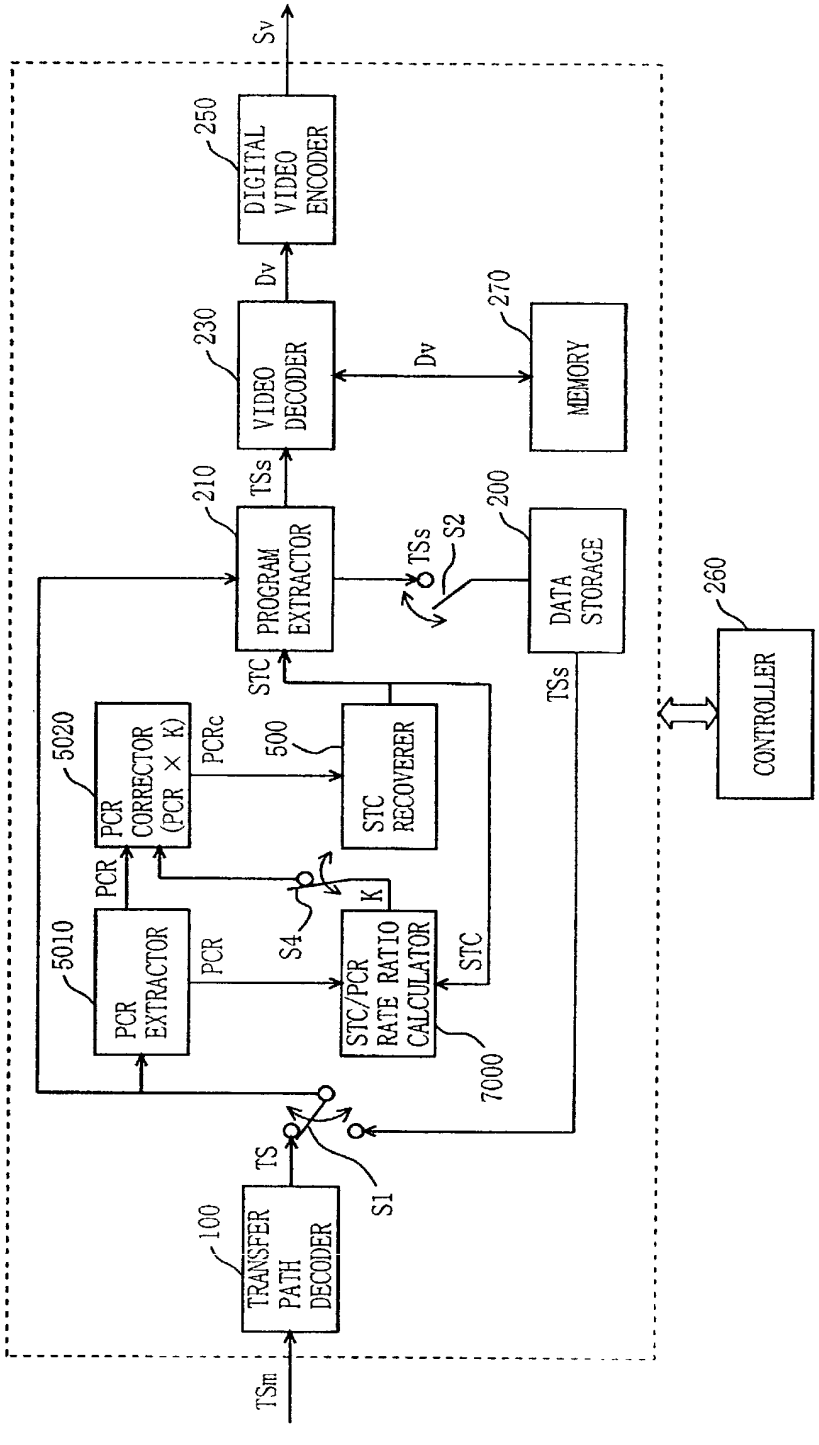

SDR3
TSm
TRANSFER PATH DECODER
100
TS
S1
PCR EXTRACTOR
5010
PCR
PCR CORRECTOR (PCR × K)
5020
PCRc
500
STC RECOVERER
STC/PCR RATE RATIO CALCULATOR
7000
K
S4
STC
PROGRAM EXTRACTOR
210
TSs
S2
DATA STORAGE
200
VIDEO DECODER
230
Dv
MEMORY
270
DIGITAL VIDEO ENCODER
250
Sv
CONTROLLER
260

FIG. 6

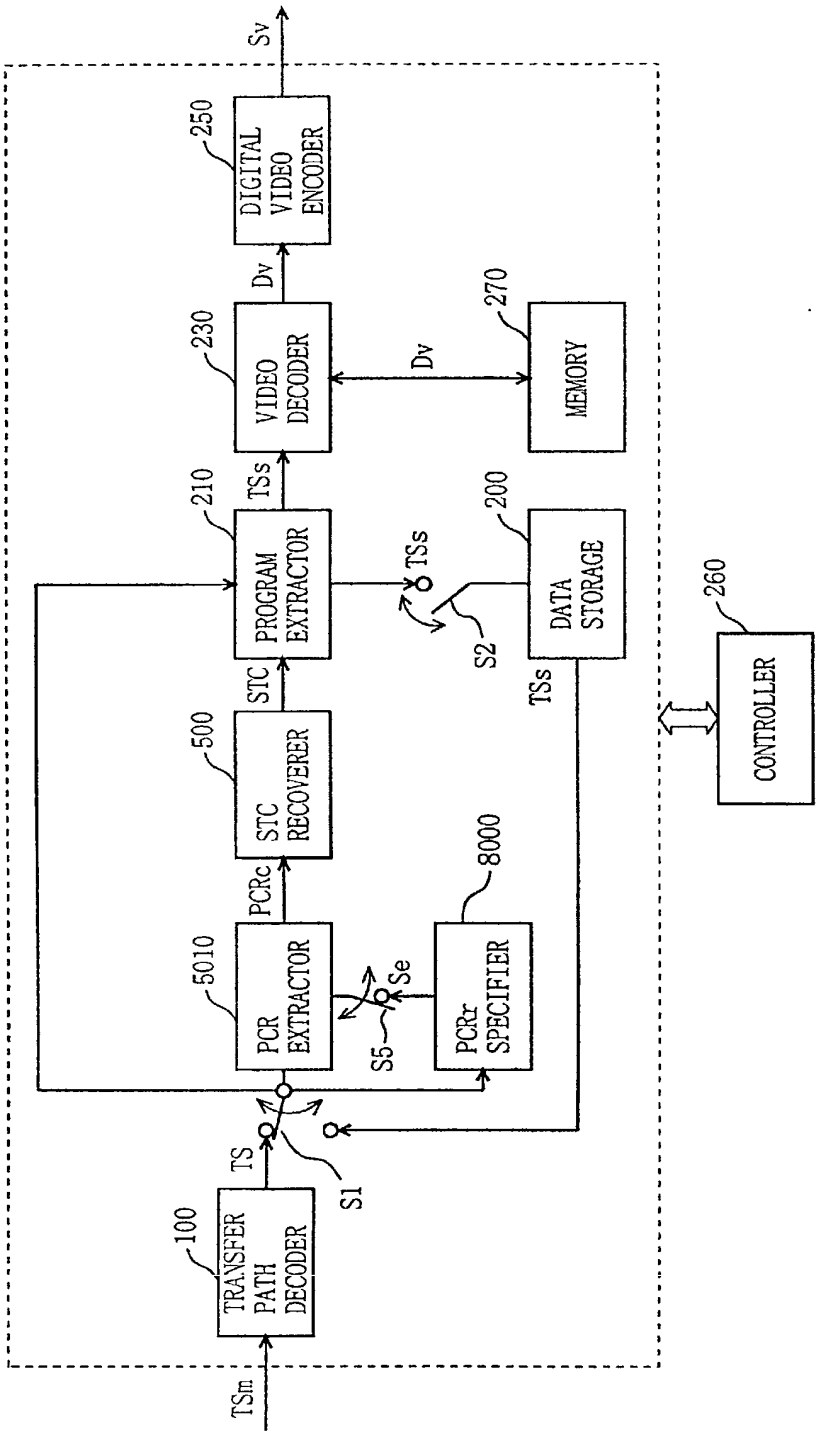
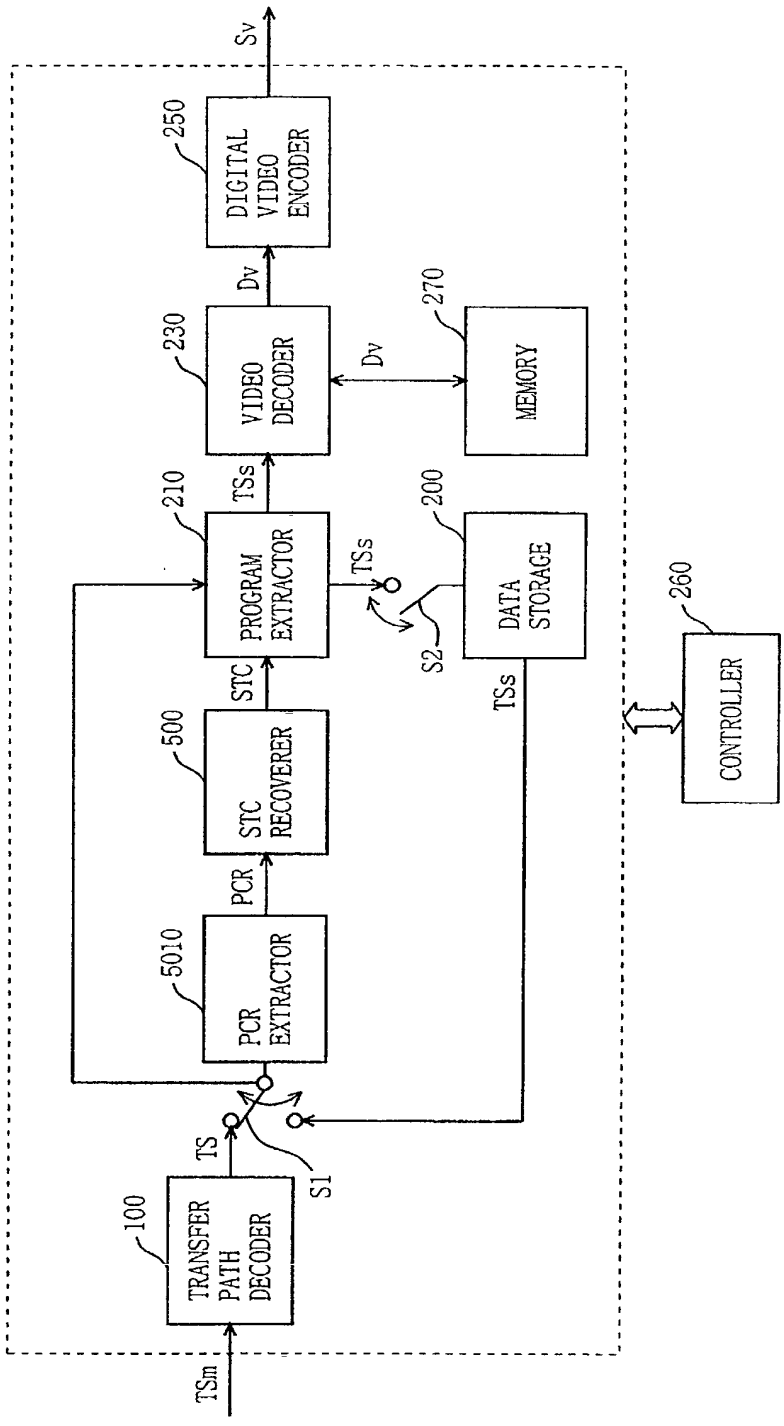
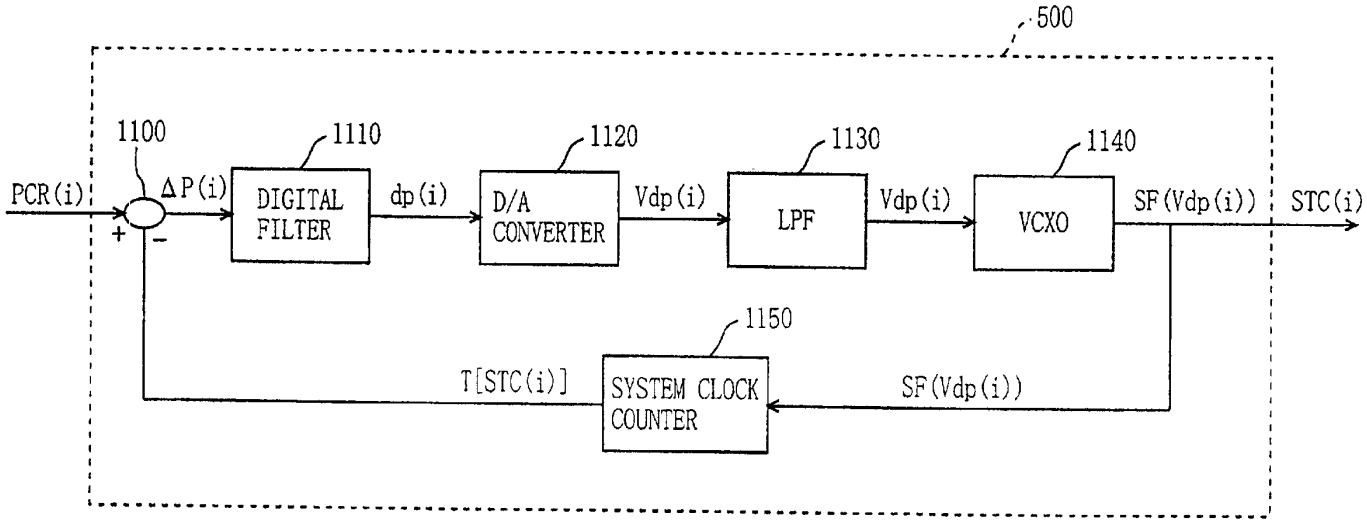

SDR4
TSm
100
TRANSFER PATH DECODER
TS
S1
5010
PCR EXTRACTOR
PCRc
500
STC RECOVERER
STC
210
PROGRAM EXTRACTOR
TSs
230
VIDEO DECODER
Dv
250
DIGITAL VIDEO ENCODER
Sv
Se
S5
8000
PCRr SPECIFIER
S2
200
DATA STORAGE
270
MEMORY
260
CONTROLLER

FIG. 7 PRIOR ART



10/018752

FIG. 8 PRIOR ART



$$T[STC(i)] = T[STC(i-1)] + Pc(i)$$

$$Pc(i) = C(Pa(i)/F(Vdp(i-1))$$

FIG. 9 PRIOR ART